H Tree 4-Spines Clock Network

FIG.1
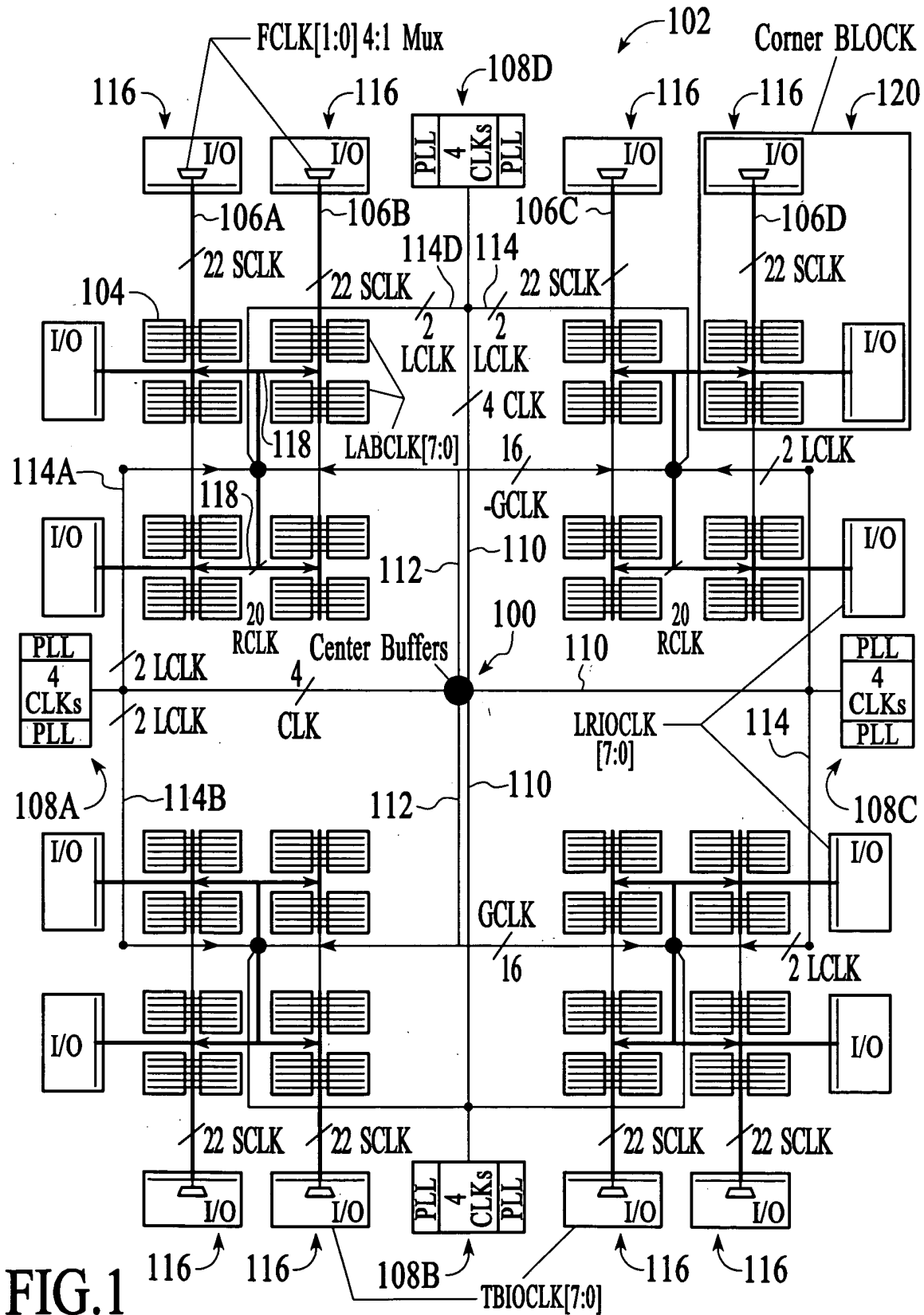
H Tree 2-Spines Clock Network
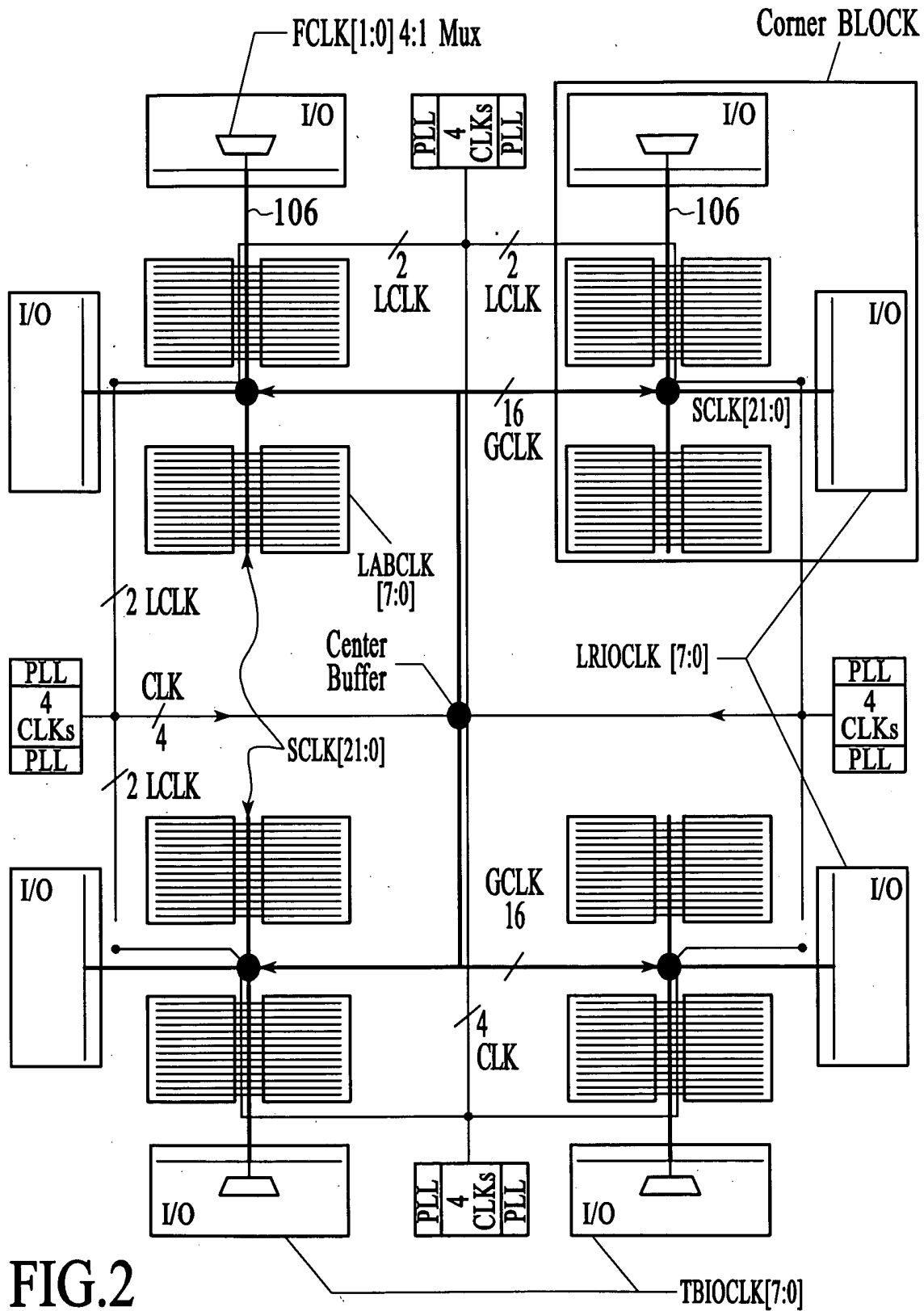
FIG.2

CORNER BLOCK for 4-Splines Clock Network
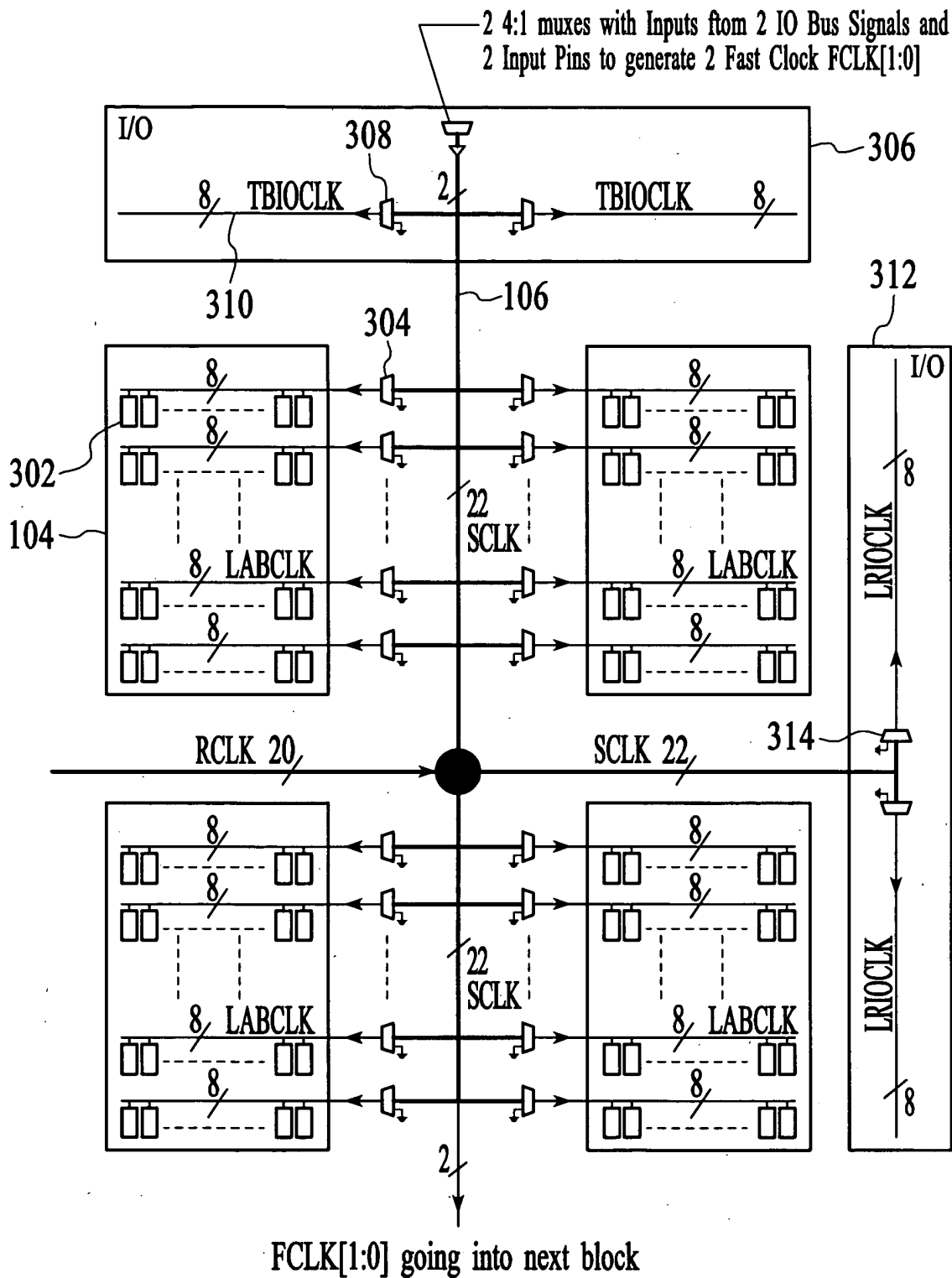
2 4:1 muxes with Inputs from 2 IO Bus Signals and
2 Input Pins to generate 2 Fast Clock FCLK[1:0]

FCLK[1:0] going into next block

FIG.3

CORNER BLOCK for 2-Splines Clock Network

2 4:1 muxes with Inputs from 2 IO Bus Signals and
2 Input Pins to generate 2 Fast Clock FCLK[1:0]

I/O

8 TBIOCLK   2   TBIOCLK   8

2 LCLK

~106

8

8

8

22 SCLK

8 LABCLK   8 LABCLK

8

I/O

8

LRIOCLK

314

GCLK 16   SCLK 22

8

8

8

8

22 SCLK

8 LABCLK   8 LABCLK

8   8

LRIOCLK

8

8

2 LCLK

FIG.4

FIG.5

GLOBAL and LOCAL Clocks Generation

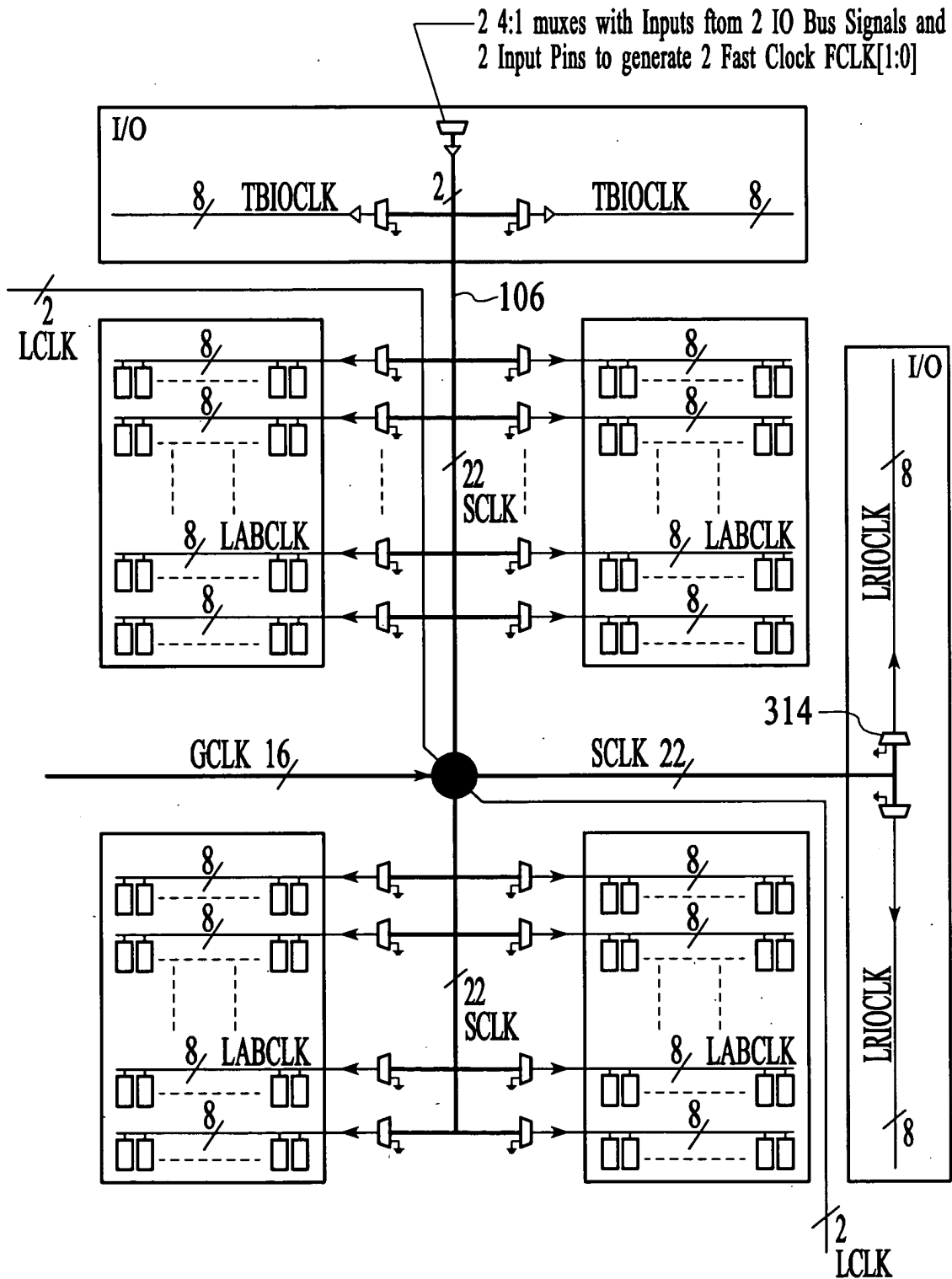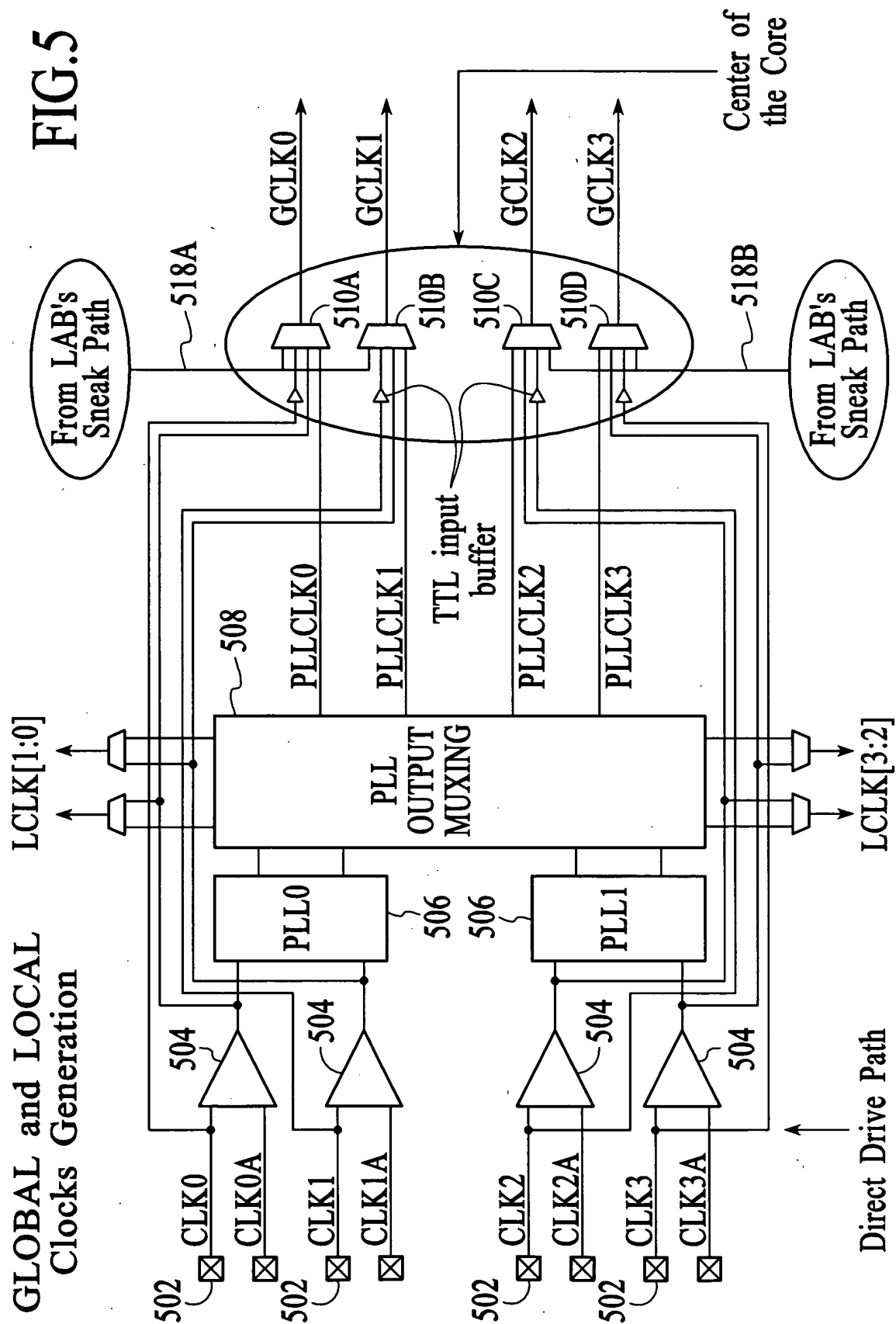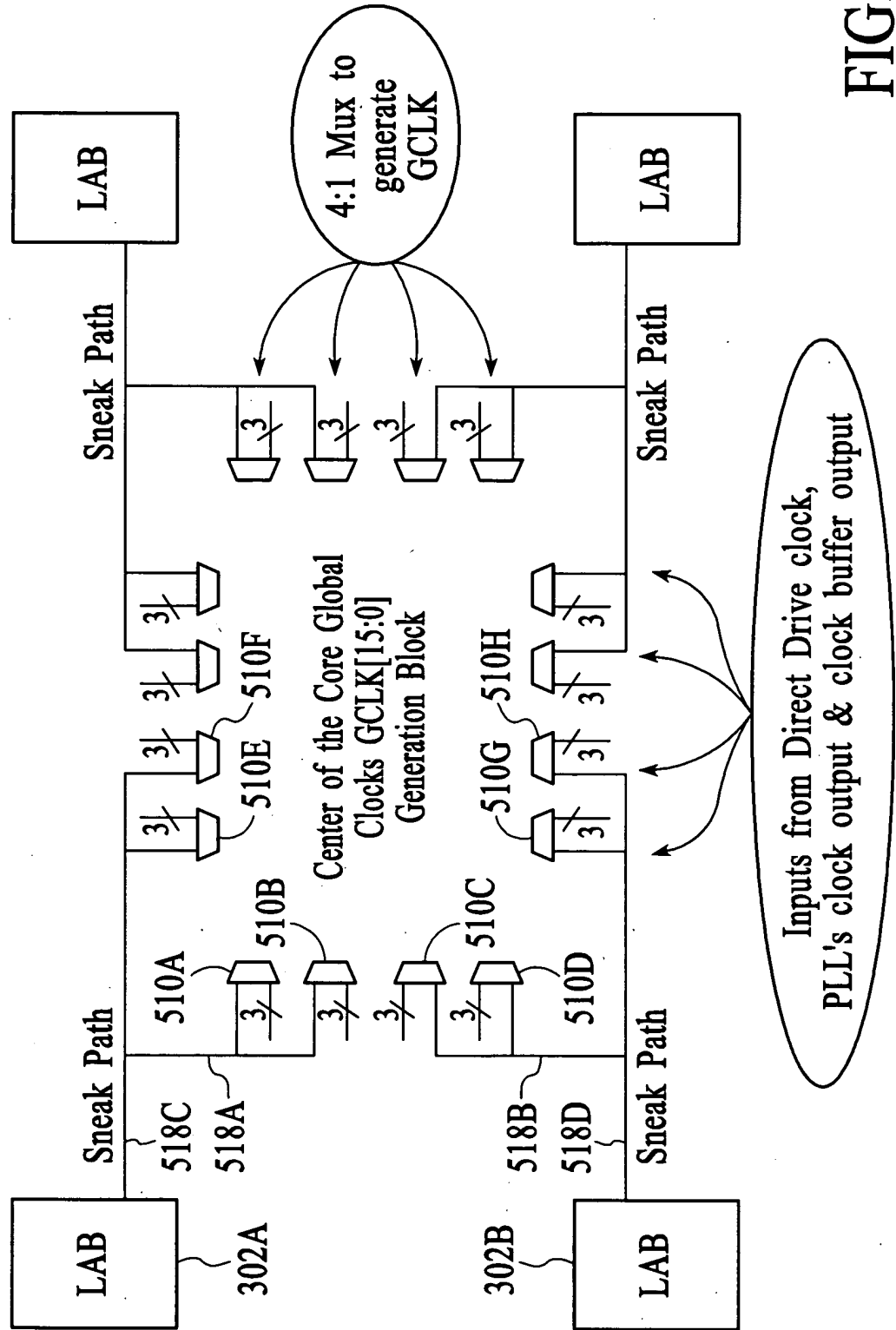Generation of Global Clocks GCLK[15:0]
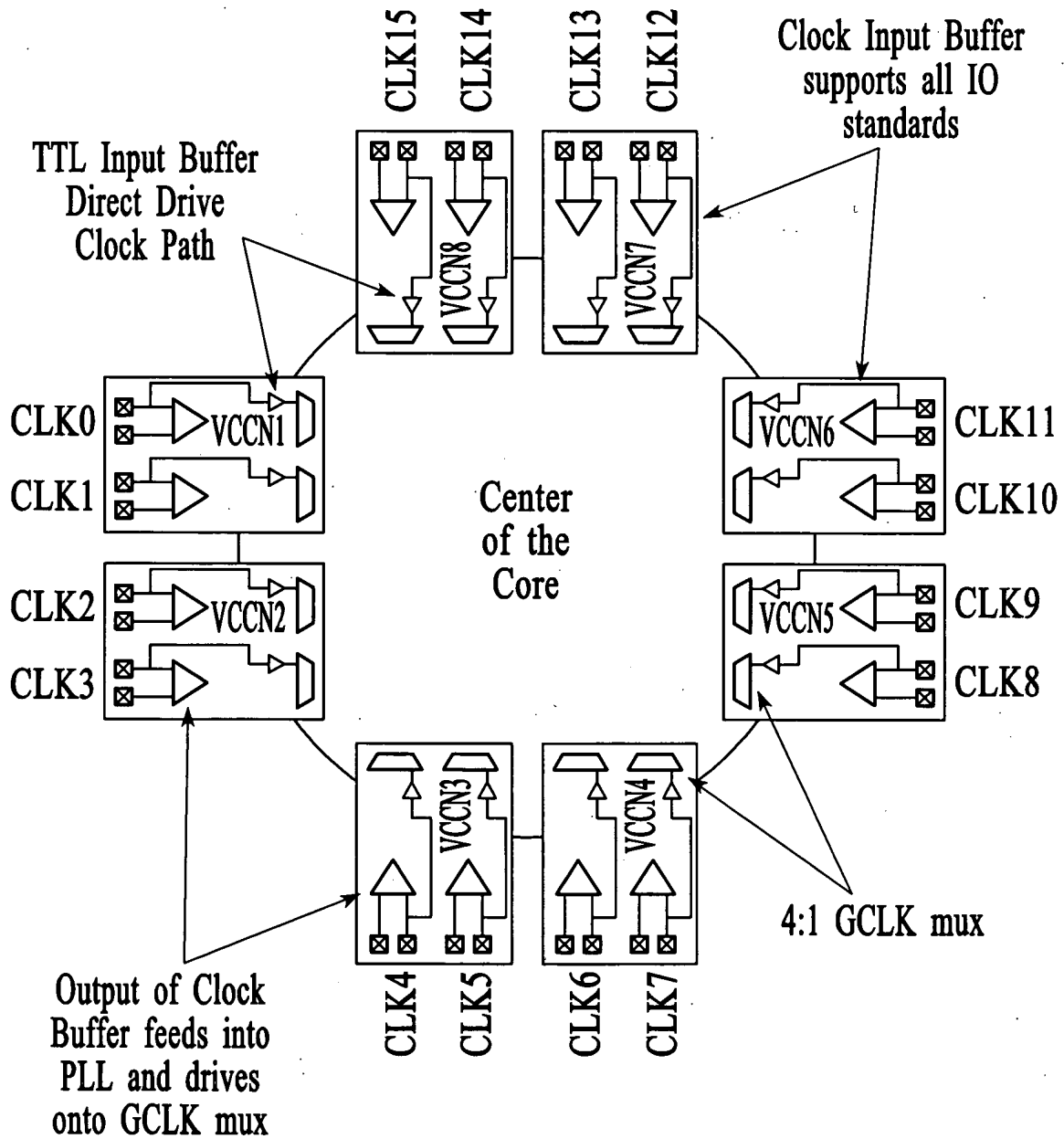

FIG.6

Power Bus Segmentation for CLOCKs

FIG.7